Amendments to the Specification

At page 1 before the "Technical Field" section, please insert the following:

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This patent resulted from a divisional application of U.S. Patent Application Serial No. 10/340,126, filed January 10, 2003, entitled "Methods of Forming Silicon-on-Insulator Comprising Integrated Circuitry, and Wafer Bonding Methods of Forming Silicon-on-Insulator Comprising Integrated Circuitry", naming Zhongze Wang as inventor, the disclosure of which is incorporated by reference; which resulted from a divisional application of U.S. Patent Application Serial No. 10/051,981, filed January 10, 2002, entitled "Silicon-on-Insulator Comprising Integrated Circuitry", naming Zhongze Wang as inventor, the disclosure of which is incorporated by reference.--

Please amend the paragraph beginning at line 3 on page 8 as follows:

Referring to Fig. 5, device wafer 10 is joined with handle wafer 20, with the preferred embodiment depicting joining device wafer 10 with silicon dioxide comprising surface 25 of handle wafer 20. Such forms a joined substrate 30. Such comprises but one preferred embodiment of an aspect of the invention. Such aspect includes a wafer bonding method of forming silicon-on-insulator comprising integrated circuitry whereby the method comprises nitridizing at least a portion of an outer surface of silicon of a device wafer. Thereafter, the device wafer is joined with the handle wafer and regardless of what subsequent processing occurs to finally form integrated circuitry. One exemplary method to bond substrate 10 with substrate 20 includes applying a suitable high voltage with opposite polarity on the device wafer and on the handle wafer. Pressing the substrates together at elevated temperature and pressure can also result in a suitable bonding. Further, by way of example only and if the oxide layer is very thin, a thermal oxidation can be conducted while pressing them together ~~a high pressure~~ <u>at high pressure</u>.

Please amend the paragraph beginning at line 19 on page 8 as follows:

The most preferred embodiment ultimately includes forming the integrated circuitry to comprise a silicon-on-insulator field effect transistor, for example and by way of example only, that depicted by Fig. 6. Fig. 6 depicts joined substrate 30 having been polished or otherwise etched back to form the depicted silicon comprising material 12 from what was the independent device wafer 10. Further thinning of joined substrate 30 can be accomplished by polishing or chemical/etching means, if desired. An exemplary thickness ~~form~~ for material 12 in Fig. 6 is from about 1000 Angstroms to about 2000 Angstroms. A pair of source/drain regions 32 and 34 ~~have~~ has been formed within silicon comprising layer 12. A gate construction 36 overlies silicon comprising layer 12 intermediate source/drain regions 32 and 34. Such is diagrammatically shown to include a gate dielectric layer 38, insulative sidewall spacers 40, and a conductive transistor gate region 41. Exemplary materials for layers 38 and 40 include silicon dioxide and silicon nitride, with exemplary materials for gate region 41 including conductively doped polysilicon and silicides.